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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,894	12/08/2003	Herman Kwong	57983.000155	9607

7590 06/05/2006

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,894	KWONG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/728,894 filed 12/08/2003 and response to election/restriction requirement filed 03/24/2006.

2. Claims 1-18 remain pending in the Application. Group II (claims 10-14) are withdrawn from a consideration as non-elected claims.

3. Applicant's election with traverse of Group I (claims 1-9 and 15-18) in the reply filed on 03/24/2006 is acknowledged. The traversal is on the ground(s) that Examiner fails to explain how the invention defined in claims 1-9 is independent from the invention defined in claims 10-14. "That is. It is clear that the invention defined in claims 1-9 and the invention defined in claims 10-14 are both directed to a method for mapping contacts of a programmable logic device (PLD) to an electronic component in a signal routing device having one or more layers (see preambles)". This is not found persuasive because Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the method for mapping contacts of a programmable logic device (PLD) to an electronic component in a signal routing device (Group I) does not require steps of optimization of the routing map (Group II) and can stand alone. The subcombination has separate utility such as **optimization** of the routing map. Moreover, the fact that the group of claims 1-9, 15-18

is disclosed in different embodiment of the specification (see specification, page 4) then the group of claims 10-14 conforms that these two groups can stand alone.

Because these inventions are distinct for the reasons given above, and the search for one group is not required for another group, restriction for examination purposes as indicated is proper.

The restriction requirement has been fully reconsidered, and is still deemed proper and is therefore made FINAL. The elected claims 1-9 and 15-18 will be examined in this office action. Claims 10-14 are withdrawn from consideration. The Applicant is advised, that cancellation of non-elected claims is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor (US Patent 5,857,109).

With respect to claim 1 Taylor teaches a method for mapping contacts of a programmable logic device (PLD) to an electronic component in a signal routing device having one or more layers within a mechanism and method for configuring a programmable logic device (PLD) and programmable connection to the PLD including

hardware resources (electronic components) connectible to the PLD (col. 4, ll.41-49), wherein PLD is mounted into PCB (col. 6, ll.34-39) and programmable logic devices, such as FPGA, PLD and CPLD are fabricated on multiple layers (col. 2, ll.27-30; col. 7, ll.47-53), the method comprising: assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device within pin assignments between PLD 11 and DRAM 13 (electronic component) as shown on the Fig. 3, wherein interconnections between PLD 11 and DRAM 13 are programmable and might be configured and reconfigured as needed, and even some of connections are fixed, pin assignments may be differencing (col. 9, ll.30-43) and wherein interconnecting PLD 11 is performed using arbitrary number of configurable channels (col. 10, ll.10-14; col. 2, ll.31-43) using bridgemode for interconnecting PLD with other electronic components, which allows flexible and variable connection through the PLD (col. 12, ll.1-2) using buses including L-bus as shown on the Fig. 3.

With respect to claim 15 Taylor teaches a signal routing device having one or more layers within PCB (col. 6, ll.34-39), wherein PLD and other electronic components are mounted to PCB and wherein mechanism and method for configuring a programmable logic device (PLD) and programmable connection to the PLD is used including hardware resources (electronic components) connectible to the PLD (col. 4, ll.41-49), and further comprising an electronic component having a plurality of contacts within electronic components (DRAM, EPROMs) having plurality of pins for connecting

with other electronic components (col. 9, ll.41-43; col. 8, ll.4-12); and a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device within creating electrically conductive traces between PLD 11 and other electronic components, such as EPROMs, DRAM etc. (col. 8, ll.4-12) within pin assignments between PLD 11 and DRAM 13 (electronic component) as shown on the Fig. 3, wherein interconnections between PLD 11 and DRAM 13 are programmable and might be configured and reconfigured as needed, and even some of connections are fixed, pin assignments may be differencing (col. 9, ll.30-43) and wherein interconnecting PLD 11 is performed using arbitrary number of configurable channels (col. 10, ll.10-14; col. 2, ll.31-43) using bridgemode for interconnecting PLD with other electronic components, which allows flexible and variable connection through the PLD (col. 12, ll.1-2) using buses including L-bus as shown on the Fig. 3; wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels within interconnecting PLD 11 is performed using arbitrary number of configurable channels (col. 10, ll.10-14; col. 2, ll.31-43).

With respect to claims 2-9 and 16-18 Taylor teaches:

Claim 2: further comprising the step of forming electrically conductive traces between the set of one or more contacts of the PLD and the respective contacts of the

electronic component accordance with the pattern of electrically conductive traces within creating electrically conductive traces between PLD 11 and other electronic components, such as EPROMs, DRAM etc. (col. 8, ll.4-12);

Claim 3: wherein one or more of the electrically conductive traces are routed to respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device within connecting PLD 11 with other electronic components within I/O channels with configurable busses (H-bus) (col. 12, ll.12-15), wherein the connection between I/) channel and the local extension of the H-bus are hardwired, but may be programmable connectible (col. 12, ll.36-38);

Claim 4: further comprising the steps determining first pattern of electrically conductive traces routed from respective contacts of the electronic component via at least one channel of the one or more channels (col. 2, ll.40-45; ll.27-30); determining a contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces (col. 9, ll.41-43); and refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second of electrically connective traces routed from the respective contacts of the electronic component via at least one of the one or more channels (col. 5, ll.54-58);

Claim 5: wherein the one or more contacts of the PLD are assigned to the one or more respective contacts of the electronic component based at least in part on the second pattern of electrically conductive traces (col. 9, ll.30-34);

Claim 6: further comprising the step of: assigning one or more contacts of the PLD to one or more respective contacts of a second electronic component of the signal routing device based at least in part on a pattern of electrically conductive traces routed from respective contacts of the second electronic component via one or more channels formed at one or more layers of the signal routing device within pin assignments between PLD 11 and DRAM 13 (electronic component) as shown on the Fig. 3, wherein interconnections between PLD 11 and DRAM 13 are programmable and might be configured and reconfigured as needed, and even some of connections are fixed, pin assignments may be differencing (col. 9, ll.30-43) and wherein interconnecting PLD 11 is performed using arbitrary number of configurable channels (col. 10, ll.10-14; col. 2, ll.31-43) using bridgemode for interconnecting PLD with other electronic components, which allows flexible and variable connection through the PLD (col. 12, ll.1-2) using buses including L-bus as shown on the Fig. 3, wherein PLD 11 mi9ght be connected to one or more electronic components, such as EPROMs, DRAM etc. (col. 8, ll.4-12);

Claim 7: further comprising the step of: assigning one or more contacts of a second PLD to one or more respective contacts of the electronic component based at least in part on a second pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device within circuit design including series of PLD and series of other electronic components as shown on the Fig. 5 (col. 2, ll.31-34), wherein interconnections between PLDs and DRAMs are programmable and might be configured and reconfigured as needed, and even some of connections are fixed, pin

assignments may be differencing (col. 9, ll.30-43) and wherein interconnecting PLD 11 is performed using arbitrary number of configurable channels (col. 10, ll.10-14; col. 2, ll.31-43) using bridgemode for interconnecting PLD with other electronic components, which allows flexible and variable connection through the PLD (col. 12, ll.1-2) using buses including L-bus as shown on the Fig. 3, wherein PLD 11 might be connected to one or more electronic components, such as EPROMs, DRAM etc. (col. 8, ll.4-12);

Claims 8 and 16: wherein the one or more contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD (col. 5, ll.1-3);

Claims 9 and 17: wherein the electronic component includes one of a group consisting of: a programmable logic device (PLD) and an application specific integrated circuit (ASIC) (col. 2, ll.1-8);

Claim 18: wherein the electrically connective traces are routed to the respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device within creating electrically conductive traces between PLD 11 and other electronic components, such as EPROMs, DRAM etc. (col. 8, ll.4-12) using channels (coo. 2, ll.40-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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